REMARKS

In the non-final Office Action, the Examiner rejects claims 1 and 2 under 35 U.S.C. § 102(e) as anticipated by TEZUKA (U.S. Patent No. 6,331,989); rejects claims 3, 11, and 13 under 35 U.S.C. § 103(a) as unpatentable over TEZUKA; allows claims 14, 15, 19, and 20; objects to claims 6 and 7 as containing allowable subject matter.

Applicant appreciates the indication that claims 14, 15, 19, and 20 are allowable over the art of record and that claims 6 and 7 would be allowable if rewritten in independent form to include all the features of the base claim and any intervening claims.

By way of the present amendment, Applicant amends claim 1 to improve form. Claims 1-3, 6, 7, 11, 13-15, 19, and 20 remain pending.

Claims 1 and 2 stand rejected under 35 U.S.C. 102(e) as allegedly anticipated by TEZUKA. Applicant respectfully traverses with respect to the claims as now amended.

A proper rejection under 35 U.S.C. § 102(e) requires that a reference teach every aspect of the claimed invention either explicitly or impliedly. Any feature not directly taught must be inherently present. See M.P.E.P. § 2131. Applicant submits that TEZUKA does not disclose or suggest the combination of features recited in Applicant's claims 1 and 2.

For example, amended independent claim 1 recites a device for directing data toward destinations. The device includes an input interface configured to receive a non-Asynchronous Transfer Mode (ATM) data stream from a single port, the non-ATM data stream including synchronous optical network (SONET) frames, identify ATM cells and Internet Protocol (IP) packets within the non-ATM data stream, and forward the ATM cells and IP packets. The device further includes a SONET deframer configured to

deframe the SONET frames in the non-ATM data stream; an IP packet forwarding facility configured to receive IP packets from the input interface, and forward the IP packets toward their destinations; and an ATM cell switching facility, where the ATM cell switching facility is separate from the IP forwarding facility and is configured to receive ATM cells from the input interface, and switch the ATM cells toward their destinations. TEZUKA does not disclose or suggest this combination of features.

For example, TEZUKA does not disclose or suggest an IP packet forwarding facility configured to receive IP packets from the input interface, and forward the IP packets toward their destinations and an ATM cell switching facility, where the ATM cell switching facility is separate from the IP forwarding facility and is configured to receive ATM cells from the input interface, and switch the ATM cells toward their destinations. The Examiner relies on TEZUKA's switch 17 as allegedly corresponding to an IP packet forwarding facility and an ATM cell switching facility (Office Action, pg. 3). Applicant respectfully submits that the disclosure of TEZUKA cannot be reasonably construed to disclose or suggest that switch 17 corresponds to an IP packet forwarding facility and a separate ATM cell switching facility, as required by claim 1.

For at least the foregoing reasons, Applicant submits that claim 1 is not anticipated by TEZUKA.

Claim 2 depends from claim 1. Therefore, this claim is not anticipated by TEZUKA for at least the reasons given above with respect to claim 1.

Claims 3, 11, and 13 stand rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over TEZUKA. Applicant respectfully traverses.

Claim 3 depends from claim 1. Accordingly, Applicant submits that this claim is

patentable over TEZUKA for at least the reasons given above with respect to claim 1. Moreover, this claim recites an additional feature not disclosed or suggested by TEZUKA.

Claim 3 recites an application specific integrated circuit (ASIC) that contains at least a portion of both the IP packet forwarding facility and the ATM cell switching facility. The Examiner admits that TEZUKA does not disclose this feature and alleges "[i]t would have been obvious to one having ordinary skill in the art to incorporate the switch of Tezuka into an ASIC to make a circuitry including the switch as compact as possible" (Office Action, pg. 4). Applicant submits that the Examiner has not established a *prima facie* case of obviousness with respect to claim 3.

The Examiner has not logically explained how implementing TEZUKA's switch 17 as an ASIC would result in a switch that is "as compact as possible." Applicant submits that the Examiner appears to have misinterpreted the feature recited in claim 3. An ASIC is a circuit designed for a specific purpose. It is unclear why the Examiner believes that implementing TEZUKA's switch 17 as an ASIC would result in a switch that is "as compact as possible."

The Examiner's motivation falls short of logically explaining why one would seek to incorporate an ASIC that contains at least a portion of both the IP packet forwarding facility and the ATM cell switching facility into the TEZUKA system. The Examiner's motivation is merely conclusory and insufficient for establishing a *prima facie* case of obviousness.

For at least these additional reasons, Applicant submits that claim 3 is patentable over TEZUKA.

Independent claim 11 recites a method that includes receiving a non-ATM data stream at one of the input ports; identifying IP packets and ATM cells in the received non-ATM data stream; directing an identified IP packet that is received on the one input port to at least one of the output ports based on an IP lookup operation; and directing an identified ATM cell that is received on the one input port to at least one of the output ports based on an ATM lookup operation, where the device includes a Synchronous Optical Network (SONET) deframer and wherein the SONET deframer is used to deframe any SONET frames in the non-ATM data stream received at the one input port. TEZUKA does not disclose or suggest this combination of features.

For example, TEZUKA does not disclose or suggest directing an identified IP packet that is received on the one input port to at least one of the output ports based on an IP lookup operation. The Examiner relies on col. 6, lines 16-25, of TEZUKA for allegedly disclosing this feature (Office Action, pg. 4). Applicant disagrees.

At col. 6, lines 16-25, TEZUKA discloses:

> According to this embodiment, one of the frame synchronization circuits 13 to 16 detects a predetermined sync pattern from one of the signals demultiplexed and output from the demultiplexing circuit 12 in the receiver, and the relationship between the outputs E to H from the demultiplexing circuit 12 and the outputs I to L is changed in accordance with the control signal output in accordance with the detection of the sync pattern. With this operation, predetermined signals can be output from desired output positions within a shorter period of time.

This section of TEZUKA is directed to detecting a predetermined sync pattern using frame synchronization circuits 13-16. Contrary to the Examiner's allegation, this section of TEZUKA in no way discloses or suggests directing an identified IP packet that is received on the one input port to at least one of the output ports based on an IP lookup

operation.

Further with respect to this feature, the Examiner alleges "detecting a predetermined sync pattern by frame synchronization circuits 13-16 is equivalent to the look-up operation" (Office Action, pg. 4). Applicant respectfully disagrees.

TEZUKA in no way discloses or suggests that frame synchronization circuits 13-16 detect the predetermined sync pattern by performing a lookup operation. Moreover, claim 11 does not simply recite a lookup operation. Instead, claim 11 specifically recites an IP lookup operation. One skilled in the art would not reasonably construe TEZUKA as disclosing that frame synchronization circuits 13-16 perform IP lookup operations to detect the predetermined sync patterns. The Examiner has not pointed to any section of TEZUKA to support the Examiner's allegation.

Claim 11 also recites directing an identified ATM cell that is received on the one input port to at least one of the output ports based on an ATM lookup operation. The Examiner appears to allege that TEZUKA's frame synchronization circuits 13-16 and switch 17 perform this feature of claim 11 (Office Action, pg. 4). Applicant disagrees.

As illustrated in Fig. 2, TEZUKA's frame synchronization circuits 13-16 detect a predetermined sync pattern from an output of demultiplexing circuit 12 (col. 6, lines 16-24). Switch 17 determines a relationship between input signals E-H and the output signals I-L, based on an "H"-level control signal R (col. 5, lines 51-53). Contrary to the Examiner's allegation, TEZUKA in no way discloses or suggests that frame synchronization circuits 13-16 or switch 17 directs an identified ATM cell that is received on the one input port to at least one of the output ports based on an ATM lookup operation.

For at least the foregoing reasons, Applicant submits that claim 11 is patentable over TEZUKA.

Claim 13 depends from claim 11. Therefore, claim 13 is patentable over TEZUKA for at least the reasons given above with respect to claim 11. Moreover, this claim is patentable over TEZUKA for reasons of its own.

Claim 13 recites that a separate ATM lookup and IP lookup is provided for each of the input ports. The Examiner did not specifically address this feature in the Office Action. Accordingly, a *prima facie* case of obviousness has not been established with respect to claim 13. Applicant respectfully requests that the Examiner specifically address the feature of claim 13 or withdraw the rejection.

For at least this additional reason, Applicant submits that claim 13 is patentable over TEZUKA.

In view of the foregoing amendment and remarks, Applicant respectfully requests the Examiner's reconsideration of this application, and the timely allowance of the pending claims.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1070 and please credit any excess fees to such deposit account.

Respectfully submitted,

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